

**REMARKS**

Claims 1-6 and 8-13 are all the claims pending in the application.

Claims 3, 5 and 8-13 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-4 and 6-13 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tang *et al.* (U.S. Patent Application Publication No. 2003/0206442 A1; hereinafter “Tang”). Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of M-Systems’ article in Home Toys E-Magazine “One Chip Does it All” (hereinafter “M-Systems”). Applicant submits the arguments below in traversal of the claim rejections.

As a preliminary matter, claims 3, 5, 8-13 comply with 35 U.S.C. § 112, second paragraph. Claim 6 has been amended to include the subject matter of claim 7. Applicant also amends claim 8 to include the subject matter of claim 12.

Applicant respectfully submits that claim 1 is patentable because each and every element of the claim is not disclosed or suggested by Tang. For example, claim 1 recites:

An apparatus for controlling execute-in-place (XIP) in a serial flash,  
comprising:

a cache module for accessing a designated memory address of the serial flash in response to a command received from a main control unit through *a system interface unit*, and reading or writing data required by the main control unit in a read or write operation;

a serial flash controller with a boot loader for allowing system booting to be performed by reading boot codes written on the serial flash, storing the boot

codes in a buffer and immediately transmitting the boot codes to the main control unit when the main control unit requires the boot codes; and

*a flash interface unit* for handling transmission and reception of data among the cache module, the serial flash controller and the serial flash.

For example, Tang fails to disclose or suggest the claimed system interface unit and the claimed flash interface unit. To anticipate a claim, “[t]he identical invention must be shown in as complete detail as is contained in the ... claim.” MPEP § 2131 *citing* Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Further, “[t]he elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required.” *See id. citing In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In the Office Action, the Examiner cites the control logic unit 320 disclosed in paragraphs 23 and 24 as corresponding to both the claimed system interface unit and the claimed flash interface unit. Because the Examiner is not able to show how Tang discloses the two separate claim elements as recited in claim 1 and because the supposedly corresponding control logic unit 320 is not arranged as required by the claims, claim 1 is believed not to be anticipated by Tang, and thus, is believed to be patentable.

Moreover, the Examiner’s characterization of the control logic unit 320 as corresponding to the claimed system interface unit and the flash interface unit is inconsistent with the Examiner’s characterization of the remaining elements of claim 1. For example, the Examiner argues that the NAND flash memory control unit 350 corresponds to the claimed serial flash controller. The NAND flash memory control unit 350, however, is part of the control logic unit

320. Again, the Examiner impermissibly points out a single component, the control logic unit 320, as corresponding to two different claim elements, the flash interface unit and the serial flash controller.

Therefore, for at least the above reasons, claim 1 is believed to be patentable.

Claims 2-4, which depend from claim 1, are patentable for at least the reasons submitted for claim 1.

In addition, claim 2 is believed to be patentable because Tang fails to disclose or suggest a cache module comprising a tag-storing unit. Although the Examiner states that the flash memory bridging device stores the data in response to a write command in Tang, there is nothing in Tang which discloses or suggests that storage information on the read page is written on the flash memory bridging device.

Claim 6 is believed to be patentable for at least the reasons submitted for claim 1.

Claim 8 is believed to be patentable because Tang fails to disclose or suggest for the operation of searching the memory address from a tag-storing unit of the controller in response to the received read command. Although Tang discloses a block address translation unit 345, this unit 345 is used for translating the logic address of the memory read instruction into an actual address corresponding to the NAND flash memory. Paragraph 26, lines 3-8. Not only is there nothing to suggest that the block address translation unit 345 is used for accessing the buffer region 310, there is nothing to suggest that the block address translation unit 345 would necessarily provide any sort of translation function to access the buffer region 310.

Therefore, claim 8 is believed to be patentable.

AMENDMENT UNDER 37 C.F.R. § 1.111  
U.S. APPLN. NO. 10/694,832

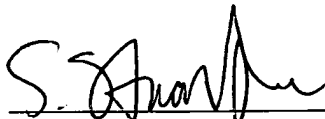
Claims 9-13, which depend from claim 8, are believed to be patentable for at least the reasons submitted for claim 8.

Claim 5, which depends from claim 1, is believed to be patentable for at least the reasons submitted for claim 1 and because M-Systems fails to make up for the deficiencies of Tang.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

  
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**23373**

CUSTOMER NUMBER

Date: January 23, 2006